NOR Gates

In this activity you will revisit the voting booth monitoring system introduced in the NAND Gates Assignment. Specifically, you will be implementing the NOR only combinational logic circuits for the two outputs ***Booth*** and ***Alarm***. In terms of efficiency and gate/IC utilization, these NOR only designs will be compared with the previously designed AOI and NAND implementations.

The truth table and K-Maps for the voting booth monitoring system can be seen in the previous NAND Gates Assignment. For your reference, the simplified logic expressions for the outputs ***Booth*** and ***Alarm*** are shown below:

$$\text{Booth} = \overline{\text{A}}\,\overline{\text{B}} + \overline{\text{C}}\,\overline{\text{D}}$$

$$\text{Alarm} = \text{A}\,\text{B} + \text{B}\,\text{C} + \text{C}\,\text{D}$$

1. In your notebook, re-draw the AOI circuits that you designed in Activity 2.2.2 NAND Logic Design.

   Booth – AOI
   Alarm – AOI

2. Re-implement these circuits assuming that only 2-input NOR gates (74LS02) are available. Draw these circuits in your notebook.

   Booth – NOR
   Alarm – NOR

3. Using Multisim, enter and test the two logic circuits that you designed. Use switches for the inputs ***A, B, C,*** and ***D*** and a probe or LED circuit for the outputs ***Booth*** and ***Alarm***. Verify that the circuits are working as expected. Print a copy of the circuit and attach it in your notebook. Note: Although the two circuits work independently, they are part of one design and should be simulated, tested, and prototyped together.

   Booth and Alarm – Multisim

4. Using the DMS breadboard, build and test the NOR logic circuits that you designed and simulated. Verify that the circuits are working as expected and that the results match the results of the simulation.

Answer the following questions in your engineering notebook:

5. For your NOR implementations, how many ICs (74LS02 chips) were required to implement your circuits? Again, we are counting ICs, not gates.
6. In terms of hardware efficiency, how does the NOR implementation compare to the AOI implementation? (Refer to the NAND Gates Assignment)
7. In terms of hardware efficiency, how does the NOR implementation compare to the NAND implementation form the NAND Gates Assignment?
8. NOR gates are available with three inputs (74LS27). Could this chip have been used for this design? If so, how would it have affected the efficiency of the design?