## Fore XOR, XNOR \& Binary Adders

## Introduction

The world's first all-transistor calculator was the IBM 608. The 608 was introduced in 1955 at a cost of $\$ 83,210$. The calculator was the size of a large dresser! The 608 was capable of addition, subtraction, multiplication, and division-the same capabilities of a four-function calculator that you can buy today at a store for $\$ 2.99$. Despite the tremendous decrease in size and price that has occurred over the last five decades, the underlying design principles for the two calculators are the same.

In this activity you will implement an adder that combines two 2-bit numbers. This 2-bit adder design is a simplified version of the adder that is in a four-function calculator. You will implement both a small-scale integration (SSI) and medium-scale integration version of the 2-bit adder.

1. Using the CDS, enter the 2-bit adder shown below. This adder is implemented with SSI logic (i.e., AND gates, OR gates, and XOR gates).


This circuit has two 2-bit inputs ( $\mathrm{X} 1, \mathrm{X} 0$ and $\mathrm{Y} 1, \mathrm{Y} 0$ ) and three outputs ( $\mathrm{S} 2, \mathrm{~S} 1$, and S 0 ). S2-S0 is the sum of adding together X1-X0 and Y1-Y0. Additionally, the outputs (S2-S0) are connected to a common anode seven-segment display through a 74LS47 display driver.

Verify that the circuit is working as expected by completing the truth table on the next page.

| INPUTS |  |  |  |  |  | OUTPUTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| X1 | X0 | X | YO | Y1 | Y | S2 | S1 | SO | Display |
| 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 | 2 |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 3 |  |  |  |  |
| 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
| 0 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
| 0 | 1 | 1 | 1 | 0 | 2 |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | 3 |  |  |  |  |
| 1 | 0 | 2 | 0 | 0 | 0 |  |  |  |  |
| 1 | 0 | 2 | 0 | 1 | 1 |  |  |  |  |
| 1 | 0 | 2 | 1 | 0 | 2 |  |  |  |  |
| 1 | 0 | 2 | 1 | 1 | 3 |  |  |  |  |
| 1 | 1 | 3 | 0 | 0 | 0 |  |  |  |  |
| 1 | 1 | 3 | 0 | 1 | 1 |  |  |  |  |
| 1 | 1 | 3 | 1 | 0 | 2 |  |  |  |  |
| 1 | 1 | 3 | 1 | 1 | 3 |  |  |  |  |

2. Using the CDS, enter the 2-bit adder shown below. This adder is implemented with 74LS183 MSI full add gates.


This circuit is functionally identical to the SSI implementation from step 1.

Verify that the circuit is working as expected by completing the truth table on the next page.

| INPUTS |  |  |  |  |  | OUTPUTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| X1 | X0 | X | YO | Y1 | Y | S2 | S1 | SO | Display |
| 0 | 0 | 0 | 0 | 0 | 0 |  |  |  |  |
| 0 | 0 | 0 | 0 | 1 | 1 |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 | 2 |  |  |  |  |
| 0 | 0 | 0 | 1 | 1 | 3 |  |  |  |  |
| 0 | 1 | 1 | 0 | 0 | 0 |  |  |  |  |
| 0 | 1 | 1 | 0 | 1 | 1 |  |  |  |  |
| 0 | 1 | 1 | 1 | 0 | 2 |  |  |  |  |
| 0 | 1 | 1 | 1 | 1 | 3 |  |  |  |  |
| 1 | 0 | 2 | 0 | 0 | 0 |  |  |  |  |
| 1 | 0 | 2 | 0 | 1 | 1 |  |  |  |  |
| 1 | 0 | 2 | 1 | 0 | 2 |  |  |  |  |
| 1 | 0 | 2 | 1 | 1 | 3 |  |  |  |  |
| 1 | 1 | 3 | 0 | 0 | 0 |  |  |  |  |
| 1 | 1 | 3 | 0 | 1 | 1 |  |  |  |  |
| 1 | 1 | 3 | 1 | 0 | 2 |  |  |  |  |
| 1 | 1 | 3 | 1 | 1 | 3 |  |  |  |  |

Answer the following questions in your engineering notebook:
3. Perform the following binary additions using your 2-bit adder:

> | 0101 | 0011 | 1001 | 1010 |
| ---: | ---: | ---: | ---: |
| +0111 | +1001 | +0101 | +1101 |

$$
\begin{array}{r}
01010011 \\
+00110110 \\
\hline
\end{array}
$$

$\begin{array}{r}01010001 \\ +01010110 \\ \hline\end{array}$

